What is claimed is:

[Claim 1] 1. A thin film transistor array plate, comprising:

a substrate, having a display region and a peripheral circuit region;

a plurality of pixel structures, disposed inside the display region;

a plurality of switching devices, disposed inside the peripheral circuit region;

a plurality of lead lines, disposed on the substrate, wherein each one of the lead lines electrically connects to the corresponding pixel structures and one of the switching devices; and

a plurality of electrostatic discharge (ESD) protection circuits, disposed inside the peripheral circuit region, wherein each one of the ESD protection circuits is electrically connected to the corresponding switching devices.

[Claim 2] 2. The thin film transistor array plate of claim 1, wherein the lead lines comprise a plurality of gate lines and a plurality of source lines.

[Claim 3] 3. The thin film transistor array plate of claim 2, wherein the ESD protection circuits comprises:

a first electrostatic discharge protection circuit, electrically connected to odd numbered gate lines;

a second electrostatic discharge protection circuit, electrically connected to even numbered gate lines;

a third electrostatic discharge protection circuit electrically connected to odd numbered source lines; and

a fourth electrostatic discharge protection circuit, electrically connected to even numbered source lines.

[Claim 4] 4. The thin film transistor array plate of claim 1, wherein the switching devices comprise thin film transistors.

[Claim 5] 5. The thin film transistor array plate of claim 1, wherein each switching device comprises at least two serially connected thin film transistors.

[Claim 6] 6. The thin film transistor array plate of claim 1, wherein each switching device comprises at least two parallel-connected thin film transistors.

[Claim 7] 7. The thin film transistor array plate of claim 1, wherein each switching device comprises at least a plurality of parallel-connected and serially connected thin film transistors.

[Claim 8] 8. A liquid crystal display panel, comprising:

a color filter plate;

a thin film transistor array plate, having a display region and a peripheral circuit region, comprising:

a plurality of pixel structures, disposed inside the display region;

a plurality of switching devices, disposed inside the peripheral circuit region;

a plurality of lead lines, disposed on the substrate, wherein each lead line electrically connects the corresponding pixel structures and one of the switching devices; and

a plurality of electrostatic discharge (ESD) protection circuits, disposed inside the peripheral circuit region, wherein each one of the ESD protection circuits is electrically connected to portions of the switching devices; and

a liquid crystal layer, disposed between the color filter plate and the thin film transistor array plate.

[Claim 9] 9. The liquid crystal display panel of claim 8, wherein the lead lines comprises a plurality of gate lines and a plurality of source lines.

[Claim 10] 10. The liquid crystal display panel of claim 9, wherein the ESD protection circuits comprises:

a first electrostatic discharge protection circuit, electrically connected to odd numbered gate lines;

a second electrostatic discharge protection circuit, electrically connected to even numbered gate lines;

a third electrostatic discharge protection circuit, electrically connected to odd numbered source lines; and

a fourth electrostatic discharge protection circuit, electrically connected to even numbered source lines.

[Claim 11] 11. The liquid crystal display panel of claim 8, wherein the switching devices comprise thin film transistors.

[Claim 12] 12. The liquid crystal display panel of claim 8, wherein each switching device comprises at least two serially connected thin film transistors.

[Claim 13] 13. The liquid crystal display panel of claim 8, wherein each switching device comprises at least two parallel-connected thin film transistors.

[Claim 14] 14. The liquid crystal display panel of claim 8, wherein each switching device comprises at least a plurality of parallel-connected and serially connected thin film transistors.

[Claim 15] 15. A thin film transistor array plate, comprising:

a substrate, having a display region and a peripheral circuit region;
a plurality of gate lines, disposed on the substrate;

a plurality of source lines, disposed on the substrate, wherein the gate lines and the source lines define the display region into a plurality of pixel areas;

a plurality of thin film transistor, each thin film transistor disposed inside one of the pixel area, wherein each one of the thin film transistors is electrically connected to one of the gate lines and one of the source lines correspondingly;

a plurality of pixel electrode, each pixel electrode positioned inside one of the pixel areas and electrically connected to a corresponding thin film transistor;

a plurality of switching devices, disposed inside the peripheral circuit region, wherein each one of the switching devices is electrically connected to one of the gate lines and the source lines;

a first electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the first electrostatic discharge protection

circuit is electrically connected to odd numbered gate lines through portions of the switching devices;

a second electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the second electrostatic discharge protection circuit is electrically connected to even numbered gate lines through portions of the switching devices;

a third electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the third electrostatic discharge protection circuit is electrically connected to odd numbered source lines through portions of the switching devices; and

a fourth electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the fourth electrostatic discharge protection circuit is electrically connected to even numbered source lines through portions of the switching devices.

[Claim 16] 16. The thin film transistor array plate of claim 15, wherein the switching devices comprise thin film transistors.

[Claim 17] 17. The thin film transistor array plate of claim 15, wherein each switching device comprises at least two serially connected thin film transistors.

[Claim 18] 18. The thin film transistor array plate of claim 15, wherein each switching device comprises at least two parallel-connected thin film transistors.

[Claim 19] 19. The thin film transistor array plate of claim 15, wherein each switching device comprises at least a plurality of parallel-connected and serially connected thin film transistors.

[Claim 20] 20. A method of preventing electrostatic discharge for the thin film transistor array plate in claim 1, the method comprising the steps of:

switching on one of the corresponding switching devices to permit the passage of any excessive electric charges accumulated on any one of the lead

lines and the subsequent redirection of those electric charges to one of the corresponding electrostatic discharge protection circuits.